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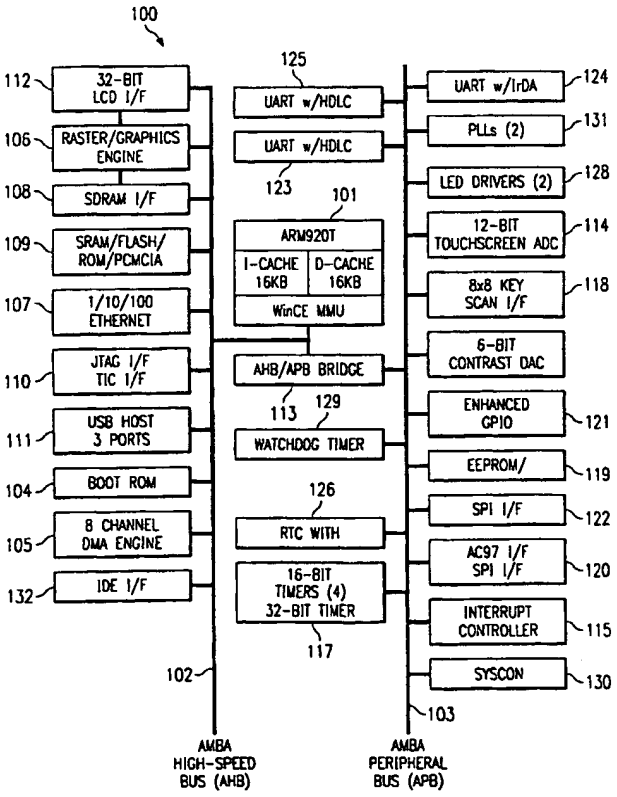
[Continued on next page]

(54) Title: A SYSTEM-ON-A-CHIP



(57) Abstract: A system (100) fabricated on a single integrated circuit chip includes a microprocessor (101) operating from a high speed bus (102) and providing overall control of the system. A peripheral bus (103) operates in conjunction with high speed bus (102) through a bus bridge (113). A first set of processing resources operate from high speed bus (102) and include a memory interface (108) for interfacing system (100) with an external memory, a direct memory access engine (105) for controlling the exchange of information between selected ones of the processing resources and the external memory through memory interface (108), and a boot memory (104) for storing boot code for initiating operation of system (100). A second set of processing resources operate from peripheral bus (103) and include an interrupt controller (115) for issuing interrupt requests to microprocessor (101) in response to selected ones of the system processing resources, a set of programmable timers (117) for generating timed interrupt signals, and a phase locked loop (131) for generating timing signals for timing selected operations of system (100).

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IPC 7 G06F15/78 G06F13/40 G06F13/28

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ALDWORTH P J: "System-on-a-chip bus architecture for embedded applications" COMPUTER DESIGN, 1999. (ICCD '99). INTERNATIONAL CONFERENCE ON AUSTIN, TX, USA 10-13 OCT. 1999, LOS ALAMITOS, CA, USA,IEEE COMPUT. SOC, US, 10 October 1999 (1999-10-10), pages 297-298, XP010360495 ISBN: 0-7695-0406-X the whole document --- -/--	1-7,9-32

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Nielsen, O

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	RINCON A M ET AL: "CORE DESIGN AND SYSTEM-ON-A-CHIP INTEGRATION" IEEE DESIGN & TEST OF COMPUTERS, IEEE COMPUTERS SOCIETY. LOS ALAMITOS, US, vol. 14, no. 4, October 1998 (1998-10), pages 26-35, XP002168633 ISSN: 0740-7475 page 28, right-hand column, paragraph 1 - paragraph 3; figure 3 ---	1,7, 10-13, 20,23, 28,29,32
X	CORDAN B: "AN EFFICIENT BUS ARCHITECTURE FOR SYSTEM-ON-CHIP DESIGN" CUSTOM INTEGRATED CIRCUITS, 1999. PROCEEDINGS OF THE IEEE 1999 SAN DIEGO, CA, USA 16-19 MAY 1999, PISCATAWAY, NJ, USA,IEEE, US, 16 May 1999 (1999-05-16), pages 623-626, XP002168630 ISBN: 0-7803-5443-5 the whole document ---	1,3,4,7, 9-32
X	CORDAN B: "EFFECTIVE MEMORY INTERFACING FOR SYSTEM-ON-CHIP DESIGNS" DESIGNCON. PROCEEDINGS OF DESIGNCON, XX, XX, vol. 5, 1 February 1999 (1999-02-01), pages 121-135, XP001009502 page 130, right-hand column -page 131, left-hand column ---	1-7,9, 11-13, 22,23
X	GARSIDE J D ET AL: "AMULET3i-an asynchronous system-on-chip" ADVANCED RESEARCH IN ASYNCHRONOUS CIRCUITS AND SYSTEMS, 2000. (ASYNC 2000). PROCEEDINGS. SIXTH INTERNATIONAL SYMPOSIUM ON EILAT, ISRAEL 2-6 APRIL 2000, LOS ALAMITOS, CA, USA,IEEE COMPUT. SOC, US, 2 April 2000 (2000-04-02), pages 162-175, XP010377325 ISBN: 0-7695-0586-4 page 165, left-hand column, paragraph 1 -page 171, left-hand column, paragraph 3 ---	1-7,9-32
A	US 6 026 443 A (KASHYAP PRAKASH ET AL) 15 February 2000 (2000-02-15) abstract -----	7,8

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6026443 A	15-02-2000	NONE	